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Simulation and Debug of Mixed Signal Virtual Platforms for Hardware-Software co-development. Vincent Motel, Cadence Design Systems, Inc. (vmotel@cadence.com) Alexandre Roybier, Cadence Design Systems, Inc. (aroybier@cadence.com) Serge Imbert, Cadence Design Systems, Inc. (sergeim@cadence.com) Abstract-Virtual platforms are often used for high level architecture exploration and hardware-software interactions verification.

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View and Analyze Simulation Results View simulation results to prototype and debug models, ...

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~~Simulation — MATLAB & Simulink — MathWorks~~ 

Vivado® Simulator is a feature-rich, mixed-language simulator that supports Verilog, SystemVerilog and VHDL language. Vivado Simulator is included in all Vivado HLx Editions at no additional cost. It does not have a design size, instances or line limitation and it allows to run unlimited instances of mixed-language simulation using single ...

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and forth through your simulation, viewing data and inspecting how and when the system changes states. For information, see [How Simulation Stepper Helps With Model Analysis](#)

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~~SimVision Debug — Cadence~~

Synopsys has announced that AIotive has adopted Synopsys VCS simulation and Verdi debug, part of the Verification Continuum Platform, to help verify its innovative aiWare hardware IP for Neural Network (NN) acceleration for automated driving applications.

~~Synopsys VCS simulation to verify automated technologies~~

Simulate mixed-signal designs with the Spectre AMS Designer/Xcelium mixed-signal

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simulators using command-line control. Learn to run simulations and debug them using the SimVision Interactive debugger. Simulate with a single-step xrun command, learn to use its associated control files.

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Mixed HDL Simulation. ModelSim combines simulation performance and capacity with the code coverage and debugging capabilities required to simulate multiple blocks and systems and attain ASIC gate-level sign-off. Comprehensive support of Verilog,

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SystemVerilog for Design, VHDL, and SystemC provide a solid foundation for single and multi-language design verification environments.

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The initialization, running, debugging and maintenance of these systems are extremely difficult tasks that, if not carefully performed, can use up the resource savings that mixed-reality simulations are designed to achieve. These issues are addressed through a set of computer applications known

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as the Mixed Reality Toolbox - or, MRT.

~~Mixed Reality Training Simulation | Virtual Reality ...~~

Multi-Core simulation which supports all design languages and constructs and either automatically or manually partitions the design to run in parallel while maintaining a single database for debug and coverage.

The theme for the 2019 conference is Novel Computing Architectures. Papers will include

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discussions on the advent of Artificial Intelligence and the promise of quantum computing that are driving disruptive computing architectures; Neuromorphic chip designs on one hand, and Quantum Bits on the other, still in R&D, will introduce new computing circuitry and memory elements, novel materials, and different test methodologies. These novel computing architectures will require further innovation which is best achieved through a collaborative Failure Analysis community composed of chip manufacturers, tool vendors, and universities.

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A Practical Guide to Analog Behavioral Modeling for IC System Design presents a methodology for abstracting an IC system so that the designer can gain a macroscopic view of how sub-systems interact, as well as verify system functionality in various applications before committing to a design. This will prevent problems that may be caused late in the design-cycle by incompatibilities between the individual blocks that comprise the overall system. This book will focus on the techniques of modelling IC systems through analog behavioral modeling and

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simulation. It will investigate a practical approach by which designers can put together these systems to analyze topological and architectural issues to optimize IC system performance. Highlights: Discussions on modeling and simulation from SPICE to behavioral simulators Comparison of various hardware description languages and a discussion on the effects of language standardization Explanation on how to reduce time-to-market by decreasing design-cycle time through modeling and simulation Contains more than 25 building block examples that can be used to construct mixed-signal IC system

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models Analysis of 4 different IC systems using various levels of model detail This book is intended for the practicing engineer who would like to gain practical knowledge in applications of analog behavioral modelling for IC system design.

Analog Circuit Design contains the contribution of 18 tutorials of the 14th workshop on Advances in Analog Circuit Design. Each part discusses a specific todote topic on new and valuable design ideas in the area of analog circuit design. Each part is presented by six experts in that field and

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state of the art information is shared and overviewed. This book is number 14 in this successful series of Analog Circuit Design, providing valuable information and excellent overviews of analog circuit design, CAD and RF systems. Analog Circuit Design is an essential reference source for analog circuit designers and researchers wishing to keep abreast with the latest development in the field. The tutorial coverage also makes it suitable for use in an advanced design course.

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Current multimedia and telecom applications require complex, heterogeneous multiprocessor system on chip (MPSoC) architectures with specific communication infrastructure in order to achieve the required performance. Heterogeneous MPSoC includes different types of processing units (DSP, microcontroller, ASIP) and different communication schemes (fast links, non standard memory organization and access). Programming an MPSoC requires the generation of efficient software running on MPSoC from a high level environment, by using the characteristics of the

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architecture. This task is known to be tedious and error prone, because it requires a combination of high level programming environments with low level software design. This book gives an overview of concepts related to embedded software design for MPSoC. It details a full software design approach, allowing systematic, high-level mapping of software applications on heterogeneous MPSoC. This approach is based on gradual refinement of hardware/software interfaces and simulation models allowing to validate the software at different abstraction levels. This book combines

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Simulink for high level programming and SystemC for the low level software development. This approach is illustrated with multiple examples of application software and MPSoC architectures that can be used for deep understanding of software design for MPSoC.

The Asia and South Pacific conference on design automation is the second in a series of biennial international conferences. It aims to provide the CAD/DA community with the opportunity to present ideas and concepts on upperstream design as well as methodologies

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of downstream design.

For Mechanical Engineering Students of Indian Universities. It is also available in 4 Individual Parts

Debugging becomes more and more the bottleneck to chip design productivity, especially while developing modern complex integrated circuits and systems at the Electronic System Level (ESL). Today, debugging is still an unsystematic and

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lengthy process. Here, a simple reporting of a failure is not enough, anymore. Rather, it becomes more and more important not only to find many errors early during development but also to provide efficient methods for their isolation. In Debugging at the Electronic System Level the state-of-the-art of modeling and verification of ESL designs is reviewed. There, a particular focus is taken onto SystemC. Then, a reasoning hierarchy is introduced. The hierarchy combines well-known debugging techniques with whole new techniques to improve the verification efficiency at ESL. The proposed systematic

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debugging approach is supported amongst others by static code analysis, debug patterns, dynamic program slicing, design visualization, property generation, and automatic failure isolation. All techniques were empirically evaluated using real-world industrial designs. Summarized, the introduced approach enables a systematic search for errors in ESL designs. Here, the debugging techniques improve and accelerate error detection, observation, and isolation as well as design understanding.

The volume presents high quality research

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papers presented at Second International Conference on Information and Communication Technology for Intelligent Systems (ICICC 2017). The conference was held during 2-4 August 2017, Pune, India and organized communally by Dr. Vishwanath Karad MIT World Peace University, Pune, India at MIT College of Engineering, Pune and supported by All India Council for Technical Education (AICTE) and Council of Scientific and Industrial Research (CSIR). The volume contains research papers focused on ICT for intelligent computation, communications and audio, and video data processing.

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